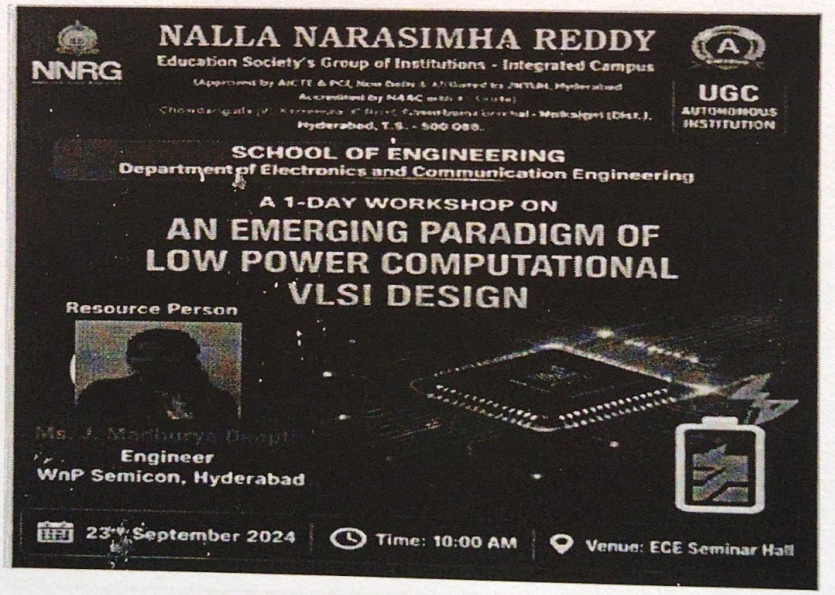
Date: 24-09-2024

# Report

on

## One Day Workshop: An Emerging Paradigm of Low Power Computational VLSI Design

| Date Organized | Title of Program | Name of Resource Person | Participants |
|---|---|---|---|
| 23/09/2024 | "An Emerging Paradigm of Low Power Computational VLSI Design" | Ms. J. Madhurya Deepti, Engineer, WnP Semicon, Hyderabad | B. Tech. ECE III (43 Students) and ECE faculty members |




### Purpose of the Program

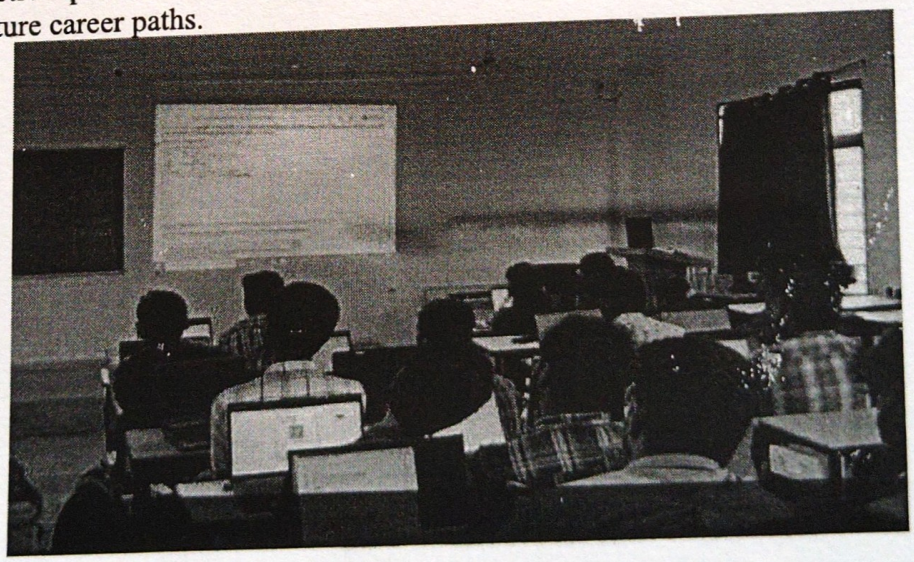
The objective of this workshop was to introduce students to advanced low-power VLSI design methodologies used in modern semiconductor industries. As energy-efficient integrated circuits have become essential for portable electronics, embedded devices, and high-performance computing systems, the workshop focused on creating awareness about power optimization techniques, CMOS scaling challenges, and modern design methodologies adopted in the VLSI industry. The program also encouraged students to explore career opportunities in semiconductor design and research.

**Day-wise Report**

The workshop commenced with an overview of VLSI technology and semiconductor industry trends. The resource person explained various sources of power dissipation in CMOS circuits and discussed dynamic and static power reduction techniques such as clock gating, power gating, multi-voltage design, and voltage scaling. Several industrial examples were presented to demonstrate the practical implementation of low-power design techniques in modern integrated circuits. The session concluded with discussions on emerging semiconductor technologies, current industry expectations, and career opportunities in VLSI design.

**Program Highlights**

The workshop featured an expert lecture by a practicing VLSI engineer from WnP Semicon, Hyderabad, providing students with first-hand knowledge of semiconductor industry practices. Real-time industrial examples, discussions on energy-efficient chip design, and explanations of modern VLSI design tools helped students understand current technological advancements. The interactive question-and-answer session enabled students to clarify technical concepts and explore future career paths.



**Outcome of the Program**

The workshop enabled students to understand the importance of low-power VLSI design in today's semiconductor industry. Participants gained knowledge of power optimization techniques, CMOS technology, and modern design methodologies used in integrated circuit development. The program improved students' analytical thinking, enhanced their awareness of industry requirements, and motivated them to pursue advanced learning and careers in VLSI and semiconductor engineering

## PO–PSO–SDG Mapping

| Program Outcomes (POs) | Program Specific Outcomes (PSOs) | Sustainable Development Goals (SDGs) |
|---|---|---|
| PO1 – Engineering Knowledge | PSO1 – Analyze VLSI Systems | SDG 4 – Quality Education |
| PO2 – Problem Analysis | PSO2 – Design Energy Efficient Systems | SDG 8 – Decent Work & Economic Growth |
| PO3 – Design & Development | | SDG 9 – Industry, Innovation & Infrastructure |
| PO5 – Modern Tool Usage | | |
| PO12 – Life-long Learning | | |

## Outcome Analysis

| Assessment Parameter | Analysis |
|---|---|
| Student Attendance | Excellent |
| Understanding of Low-Power Concepts | Improved considerably |
| Industry Awareness | Enhanced through expert interaction |
| Learning Effectiveness | High due to practical examples and case studies |
| Student Feedback | Positive and encouraging |
| Overall Success | The workshop successfully achieved its learning objectives |

## Overall Impact

The workshop significantly improved students' understanding of low-power computational VLSI design and semiconductor technologies. It strengthened their analytical skills, increased awareness of current industrial practices, and motivated them to pursue careers and research in VLSI and semiconductor engineering.

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